

In the Drawings:

The attached sheet of drawing includes changes to Fig. 5. An Annotated sheet showing the changes is attached along with the Replacement sheet.

## **REMARKS**

As a preliminary matter, Applicants appreciate the Examiner's indication of allowable subject matter contained in claims 2-6 and 10-14 if rewritten to overcome the rejections under §112. As a further preliminary matter, claims 3, 5-6, 11 and 13-14 are amended to define the acronym "LBA" as a "logical block address" in the claims. Accordingly, withdrawal of the objection to these claims is respectfully requested.

As a further preliminary matter, FIG. 5 is amended to correct grammatical errors.

Claims 1-9 stand rejected under 35 U.S.C. 112 as being indefinite. In response, Applicants amended independent claims 1-9 to clarify that the I/O request is for one logical unit of a plurality of logical units, and that the another I/O request is for another logical unit of the plurality of logical units, and also that the concatenation logical unit is out of a plurality of controllers which shares the plurality of logical units. For these reasons, withdrawal of the §112 rejection is respectfully requested.

Claims 1, 7-9 and 15-16 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' Admitted Prior Art (AAPA) in view of Nunnelley et al. (U.S. Patent No. 5,423,046). In response, Applicants amended the claims to clarify that the channel adapter of a received controller creates two I/O requests from a single I/O request of a host upon detecting an access to a concatenation logical unit, and respectfully traverse the rejection as it applies to the amended claims.

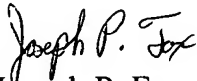
As discussed in Applicants' specification page 16, line 8 *et seq.*, when a host 3 specifies I/O access to a logical block address range corresponding to a logical unit LU 0 within a concatenation LU 0, the CA 11 the first to a CA control table 50 and determines a logical unit LU 0 in-charge from the I/O start logical block address and determines the CM 20 in-charge from the determined LU 0. The CA 11 sends the I/O data request to the CM 20. (See FIG. 9). Furthermore, as shown in FIG. 10, when a host 3 specifies I/O access to the logical block address range corresponding to the logical unit LU 1 within a concatenation LU 0, the CA 11 refers to the CA control table 50 and determines the logical unit LU 1 n-charge from the I/O start logical block address, and determines CM 30 n-charge from the determined LU 1. The CA 11 sends a I/O data request to the CM 30.

The AAPA, however, merely discloses a concatenation process except for sending a I/O request to another controller in charge of another logical unit constituting a concatenation logic unit, which is described in the present application. Similarly, Nunnelley merely discloses a parallel access process that sends I/O requests to a plural controller when accessing a database from a cluster. Accordingly, both the AAPA and Nunnelley fail to disclose or suggest the channel adapter of a receive controller that creates two I/O requests from a single I/O request of a host when detecting an access to a concatenation logical unit. For this reason, Applicants respectfully request withdrawal of the §103(a) rejection of claim 1, 7-9 and 15-16.

For all of the foregoing reasons, Applicants submit that this Application is in condition for allowance, which is respectfully requested. The Examiner is invited to contact the undersigned attorney if an interview would expedite prosecution.

Respectfully submitted,

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FIG. 5

